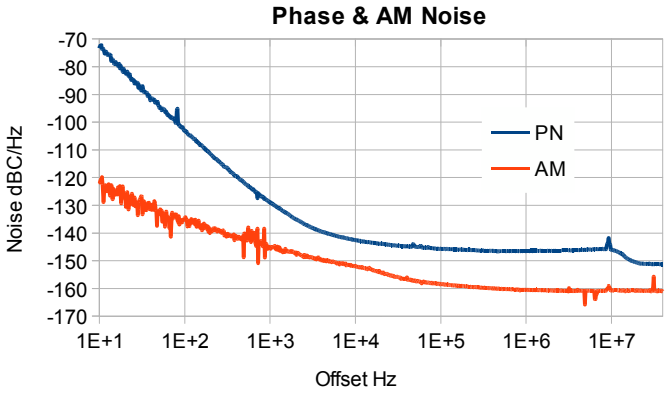
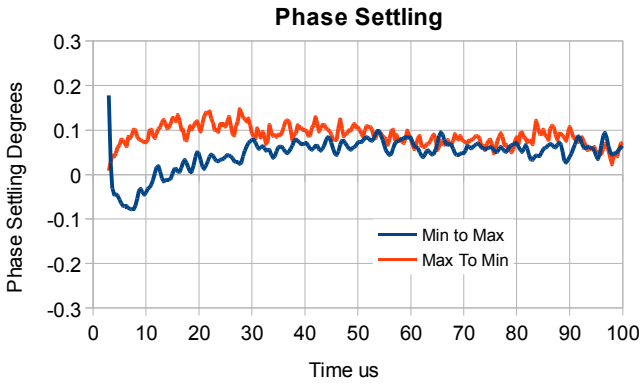
Frequency Agile Low Noise Local Oscillator

Pascall Electronics S-Band Frequency Agile Local Oscillator has been designed to meet the low phase noise and fast phase settling requirements of the latest generation of land and sea based multifunction surveillance radars.
The high output level leaves ample power available even after signal distribution. A test output is provided for system maintenance and monitoring without interruption to the main output signal.
High frequency accuracy and 16 bit resolution help to simplify spectrum management issues where rapid deployment is necessary.
User defined control features allow the output frequency to follow the input control word or for changes to be synchronised to the rising or falling edge of a trigger pulse.
While being designed for use in current and future systems, these flexible features enable easy integration into existing systems bringing up to date performance to aging hardware.



Phase and amplitude noise measured using an Agilent E5052B signal source analyser



Phase settling to and from frequency extremes

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S Band Frequency Agile Local Oscillator Specification

Frequency range	3550 to 4150MHz	
Number of channels	65535	
Channel selection code	16 bits binary 0x0000 represents lowest frequency, 3550MHz 0xFFFF represent highest frequency, 4150MHz	
Control interface	differential TTL	
Output return loss	17dB max	
Output power Main O/P	27dBm ±1.5dB	
Output power Test O/P	Main O/P -20dB Nominal	
Frequency accuracy	±2 ppm max	
Long term stability	±0.5 ppm per year max	
Vibration sensitivity	1E-9/g max	
Phase noise (max)	10Hz 100Hz 1kHz 10kHz 100kHz >=1MHz	-53dBc/Hz -87dBc/Hz -120dBc/Hz -133dBc/Hz -140dBc/Hz -143dBc/Hz
Amplitude noise (max)	10Hz 100Hz 1kHz 10kHz 100kHz >=1MHz	-103dBc/Hz -115dBc/Hz -120dBc/Hz -130dBc/Hz -140dBc/Hz -150dBc/Hz
Spurious outputs Non harmonic Harmonics	 -80dBc max 2^{nd} -60dBc max >2^{nd} -80dBc max	
Switching speed Amplitude settling Phase settling	±0.5dB max 1us after channel change ±0.1dB max 5us after channel change ±0.3deg max 10us after channel change	
Built in test	Differential TTL Fail indicated for low output level. Transition region, 22 to 18dBm	
Operating Temperature	0 to 60ºC min	
Power supply See ordering info	48V isolated, 2 Amps 24V isolated, 4 Amps 15V isolated, 6.5 Amps	
Size (w x h x d)	210 x 170 x 320mm	

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User Interface:

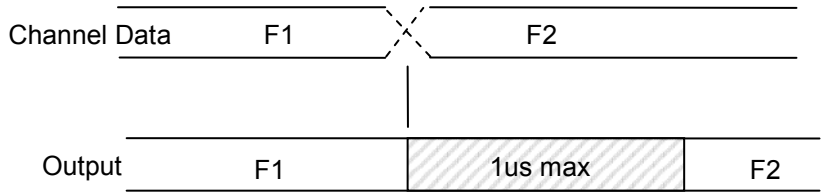
RF O/P connectors	SMA Jack
Power Supply Input	6 way MIL-C-38999 17-6 plug Orientation N
Data Connector	55 way MIL-C-38999 17-35 socket Orientation D

Channel change control

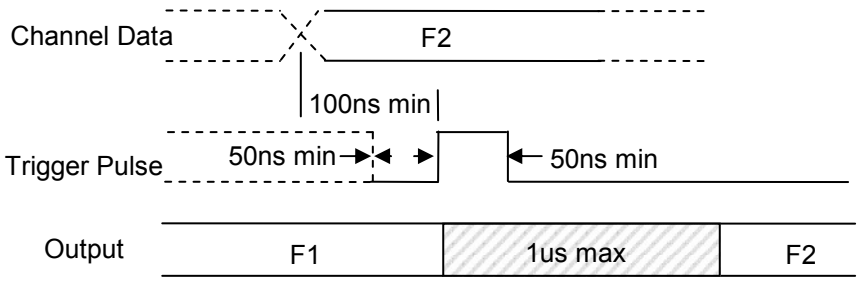
The channel change method is controlled by user configurable links accessible on the data connector. If Trigger Enable is left open circuit the output channel is defined by the current state of the channel select code input lines. Shorting the Trigger Enable link causes channel changes to be initiated by a trigger pulse whose polarity can be selected by the state of the Trigger Polarity link.

Link	Short	Open
Trigger Enable	Channel change on trigger edge	Channel change on data change
Trigger Polarity	Change on falling edge	Change on rising edge

Channel change options



Trigger Enable Open Circuit



Trigger Enable Short Circuit, Trigger Polarity Open Circuit

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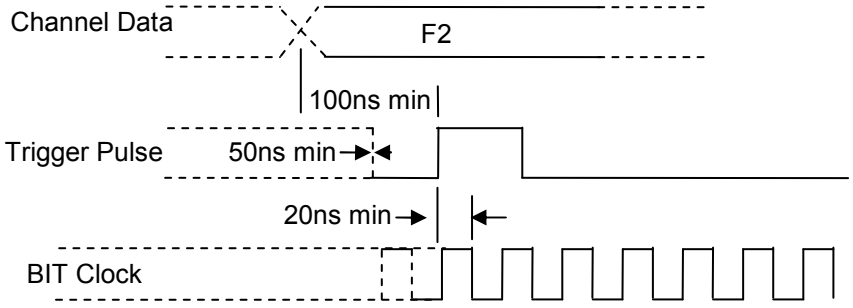
Built In Test (BIT)
The STALO has a single BIT output to indicate the correct operation of the unit. This can be reconfigured as a serial output that also includes a tell back of the Channel Select Code by linking together the Serial BIT pins. This feature can only be used if edge triggering is enabled. A differential serial clock input of up to 10MHz is required and the timing of the trigger pulse must be such that the pulse encompasses at least one negative going clock edge. The serial clock must be enabled for at least 700 cycles after the trigger edge of the channel change pulse to ensure that the BIT data can be successfully received. The data format for each byte is 8 data bits, even parity and 1 start & 1 stop bit.
There are three data bytes following each other consecutively containing the following data:
Byte 1 Channel Selection Code MSB tell back
Byte 2 Channel Selection Code LSB tell back
Byte 3 BIT.



BIT Clock with positive edge Trigger

Ordering information

SFG – 48	48V PSU Supply Voltage
SFG – 24	24V PSU Supply Voltage
SFG – 15	15V PSU Supply Voltage

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