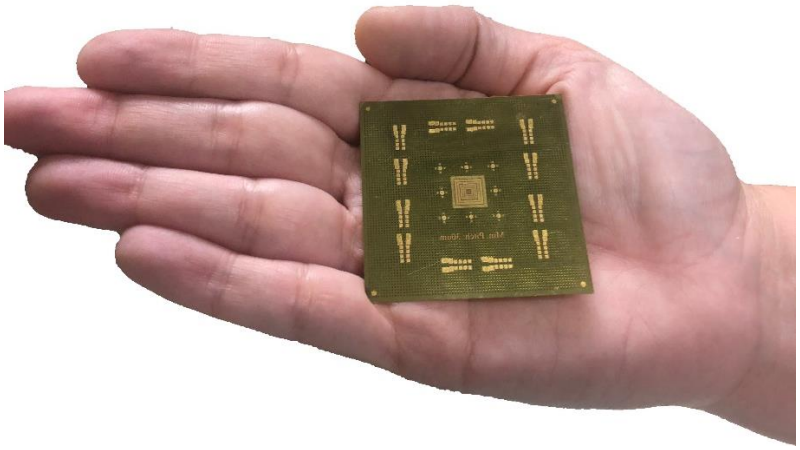
News Release: 50µm pitch Chiplet substrates from Paricon Technologies now available



shown above is Chiplet substrate with 8,000 contact pads.

Paricon Technologies announces the availability of multilayer polyimide substrates used in Chiplet packaging, or device-testing space transformers.

The typical pitch on the wafer side of the substrate is about 50 µm. The typical pitch on the PCB side is about 0.5mm.

The substrates typically have 10 routing layers and measure up to 50mm x 50mm.

The pads, traces, and vias are copper.

The polyimide dielectric constant is 2.9 and the CTE is 3 ppm/°K.

Chiplet Substrate Information

Laminate Material	Polyimide
Trace/Pad Material	Copper
Size	up to 50mm x 50mm
Thickness	typically 100µm - 200µm
Mounting	can be mounted on a ridged carrier
Manufacturing method	Additive
Trace/Space	5µm/5µm
Vias	10µm
Layers	up to 10
Pitch on IC side	typically 50µm
Pitch on PCB side	Range: 0.4mm – 1.0mm
Temperature rating	270°C
CTE	3ppm/K
Dielectric constant	2.9
Young's Modulus	100-200GPa
Multilayer routing	from 4 – 10 Controlled impedance possible with ground planes
Continuity testing	each substrate is 100% continuity tested on an ATF flying head PCB tester

Lead times		
	1) Define the specifications of the substrate	pre-sale
	2) Customer makes a net list (a wiring to-from list)	1 week
	3) Route the traces through the layers (software)	3 weeks
	4) Customer approval of routing in layers	1 week
	4) Manufacture the production masks	1 week
	5) Manufacture the multilayer substrates	5 weeks
	6) Do a continuity test	1 week
	Total	12 weeks

For more information, please contact Bernd.Rupp@RUPPtronik.de or Paricon Technologies